A CONVENIENT MULTIPLEXING SCHEME FOR ADDRESSING SMALL LIQUID CRYSTAL MATRIX
DISPLAYS

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In this paper, a convenient method for multiplexing small liquid crystal matrix
displays is presented. For a matrix of N rows, the method consists of address-
ing the rows with all possible combinations of a binary voltage scheme. For
each of these 2^N combinations, a proper binary voltage is selected for each of
the columns to get a majority-advantage compared to the picture pattern to be
displayed. A mathematical analysis of this scheme is given. Though the con-
trast ratio with the present scheme is slightly less than that obtained with
the conventional scheme it has the advantage of having a very large duty factor and
of requiring only one power supply. The simplicity of the scheme is exploited
to construct and operate a 16-segment alphanumeric display panel.

INTRODUCTION

For many low cost, high volume type of applications, it would be useful to
have relatively cheap, multiplexed alphanumeric liquid crystal displays (LCDs).
We have tried to develop such a display with simple circuitry.

THE MULTIPLEXING SCHEME

From the practical point of view, it is an extremely simple matter to
generate a sequence of binary numbers using a counter. We have made use of
this facility in developing an addressing scheme suitable for LCDs.

Consider a matrix with N rows. For reasons which will be obvious soon,
let N be an odd number. If, as usual, 1 stands for 'high' and 0 for 'low'
voltages (positive logic) a total of 2^N different signals (which are the
possible N-bit binary numbers) can be applied to the N rows. With each of
these possible voltage-patterns on the rows, we will apply such a voltage
to a given column that the error with reference to the required pattern is
minimised. This is illustrated in Fig.1 for a matrix with 5 rows. In general,
if '1' is $+V_r$ and '0' is $-V_r$ on the rows, we can apply either $+V_c$ or $-V_c$ to
the columns. Only the RMS voltage is relevant to the electro-optic response
of the LCD and at any given time the squared voltage on any given element is
$(V_r+V_c)^2$ or $(V_r-V_c)^2$. It is not necessary to consider all the 2^N possible
binary numbers applied to the rows, since one half of them will be comple-
mentary to the other half (see fig.1). Let us assume that a given element
in a given column should be 'ON'. The RMS voltage on that element can be
calculated as follows: Let P be the number of times that the element has a
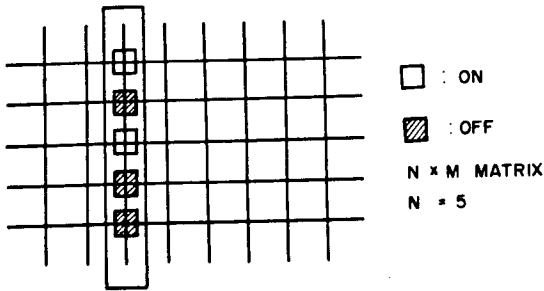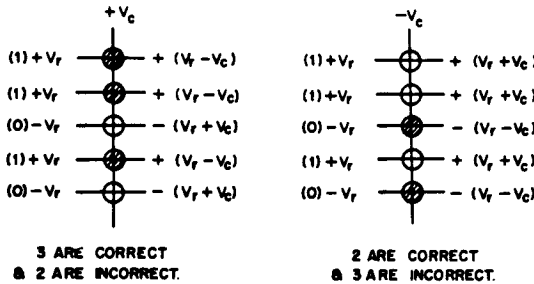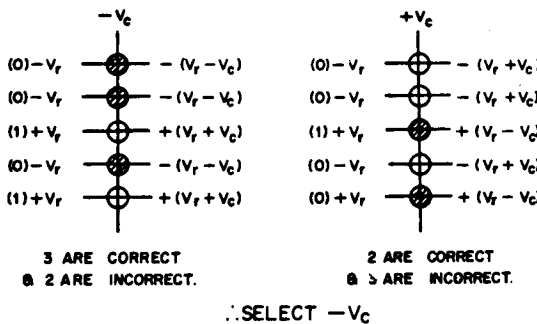squared voltage equal to $(V_r+V_c)^2$. In the remaining number of scans, viz.,

Figure 1.

(a) Schematic diagram of a matrix with 5 rows. The required picture-pattern of only one column is shown.

$N \times M$ MATRIX

$N = 5$

(b) Illustration of the scheme of selection of the row and column voltages used to reproduce the picture elements shown in Fig.1(a). In the upper section of the figure, the binary number defining the voltages applied to the rows is 11010. $+V_c$ is selected as the column voltage to minimise the errors. In the lower section of the figure, the rows get voltages corresponding to the binary number 00101 (i.e., complementary to 11010), with $-V_c$ selected for the column. Notice that in the complementary scan the polarities of the voltages on all the picture elements are reversed.

$(2^{N-1}-P)$ scans, that element will have a squared voltage equal to $(V_r-V_c)^2$. Only <u>once</u> during the 2^{N-1} scans, <u>all</u> the elements of the given column will have the correct voltages (i.e., 'ON' elements have $(V_r+V_c)^2$ and 'OFF' elements have $(V_r-V_c)^2$). There will be <u>one</u> mistake in <u>N</u> out of the 2^{N-1} scans. However, we want the given element to be 'ON'. So, in $(N-1)$ scans the given element is 'ON' when the picture-pattern in the given column has one mistake. This can also be written as $(N-1)!/1!(N-2)!$ which is the number of ways of selecting one out of $(N-1)$ elements of the column.

In a similar manner, when there are two mistakes in the picture-pattern, excluding the cases where the given element has a mistake, the number of times it is 'ON' is $(N-1)!/2!(N-3)!$.

We can continue this series till we reach the maximum possible error. By choice, this error cannot exceed $(N-1)/2$. The counting procedure is illustrated for $N = 5$ in figure 2.

$$\frac{(5-1)!}{0!(5-1-0)!} = 1 \qquad\qquad \frac{(5-1)!}{1!(5-1-1)!} = 4$$
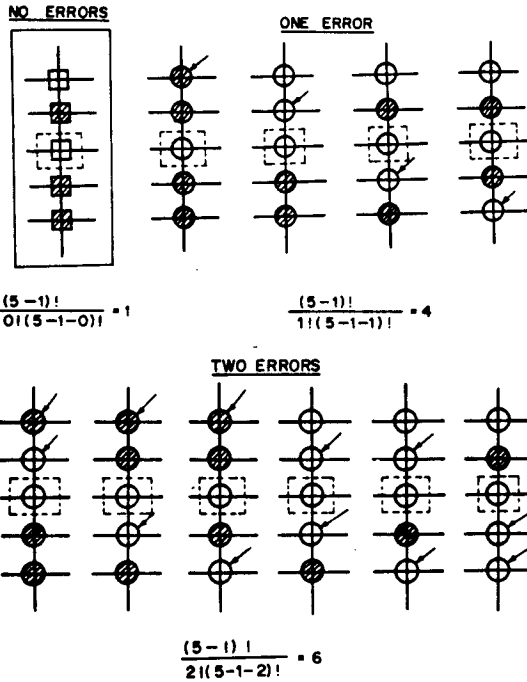
$$\frac{(5-1)!}{2!(5-1-2)!} = 6$$

Figure 2.

Illustration of the method of counting the number P (as defined in the text) for a matrix with 5 rows. The central picture element (enclosed in a box with dashed lines) of the column shown in fig.1(a) is chosen for the purpose of calculating P. The arrows indicate errors compared to the pattern in fig.1(a).

Hence the total number of scans for which an 'ON' element has $(V_r+V_c)^2$ as the squared voltage is given by

$$P = \sum_{m=0}^{\frac{N-1}{2}} \frac{(N-1)!}{m!\,(N-1-m)!} \tag{1}$$

In the remaining $(2^{N-1}-P)$ scans, the element has $(V_r-V_c)^2$ as the squared voltage. Hence the RMS voltage on the 'ON' element is

$$V_{ON}(RMS) = \left[\frac{P(V_r+V_c)^2+(2^{N-1}-P)(V_r-V_c)^2}{2^{N-1}} \right]^{\frac{1}{2}} \tag{2}$$

In a similar manner,

$$V_{OFF}(RMS) = \left[\frac{P(V_r-V_c)^2+(2^{N-1}-P)(V_r+V_c)^2}{2^{N-1}} \right]^{\frac{1}{2}} \tag{3}$$

It can be easily shown that V_{ON}/V_{OFF} is optimised for $V_r = V_c$. Then

$$V_{ON}/V_{OFF} = \sqrt{P/(2^{N-1}-P)} \tag{4}$$

Let $V_r = V_c = V$. In fact we can chose '1' to be 'V' and '0' to be zero itself. Thus a single source of voltage is adequate to address the display. Further, when we scan through the complementary 2^{N-1} binary numbers, any given element will get an equal number of voltage pulses of opposite sign, so that a DC-free operation is automatically ensured (see also fig.1).

When N is even, it is clear that the choice of the voltage to be applied to the column electrode becomes ambiguous when N/2 mistakes occur for a given voltage-pattern on the row-electrodes. Covering both the possibilities is equivalent to scanning a matrix with (N+1) rows, i.e., eqn.(4) holds good with N replaced by N+1.

It is also clear that since a total of 2^N scans are needed to cover all possibilities, the number of scans rapidly increases with N. Hence this method of addressing is useful only for small matrices.

The optical contrast ratio depends on the RMS value of (V_{ON}/V_{OFF}). It is listed below for a few values of N and compared with the values for the conventional scanning method due to Alt and Pleshko[1].

RMS value of (V_{ON}/V_{OFF})

	Present method R_P	Alt and Pleshko R_{AP}	R_{AP}/R_P
N = 3	1.732	1.932	1.115
N = 5	1.483	1.618	1.091
N = 7	1.382	1.488	1.077
N = 9	1.324	1.414	1.068

Hence the Alt and Pleshko values are always higher than the ones got by the present method. However, as N increases the two values approach each other.

Nontheless, in view of the advantages of the new method, viz., (a) need for a single voltage source, and (b) DC-free operation, we have used it in addressing a 16-segment alphanumeric display. An additional advantage is that since, in the present method, an ON element is 'ON' most of the time (i.e., it has a relatively 'large' duty factor) a flicker-free operation is ensured even with relatively low scanning rates. (This may be compared with the duty factor of 1/N in the conventional method).

We very recently came across a paper by Clark et al[2] in which they appear to have considered a similar multiplexing technique. By using the results of a computer simulation analysis, they have conjectured that

$$V_{ON}/V_{OFF} = \left[1+\left\{\frac{2^{2q-1}}{\binom{2q}{q}} - \frac{1}{2}\right\}^{-1}\right]^{\frac{1}{2}} \qquad (5)$$

where q is an integer, N = 2q+1 and $\binom{2q}{q}$ denotes a binominal coefficient. By using binominal series, it can be easily shown that (4) reduces to (5). Thus our mathematical analysis confirms the conjecture by Clark et al.
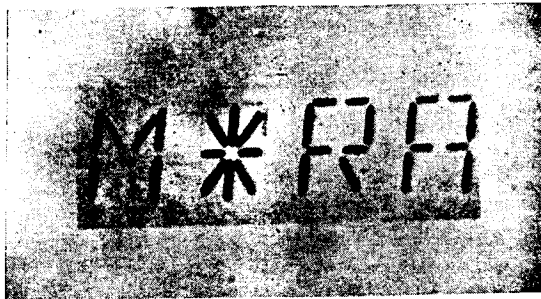
16-SEGMENT ALPHANUMERIC DISPLAY

We treat each character as a 4 × 4 matrix. The interconnections on the top and bottom plates are shown in figure 3.

Since we did not have a standard character generator IC for addressing such a display, a 1702EPROM was programmed to convert the ASCII code from a key board
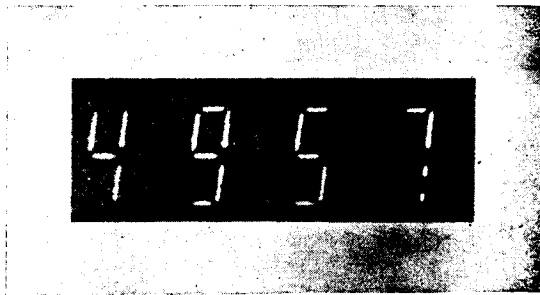
a

b

Figure 5   Photographs of two alpha-numeric patterns of a TN display panel with (a) parallel polarizers and (b) perpendicular polarizers.
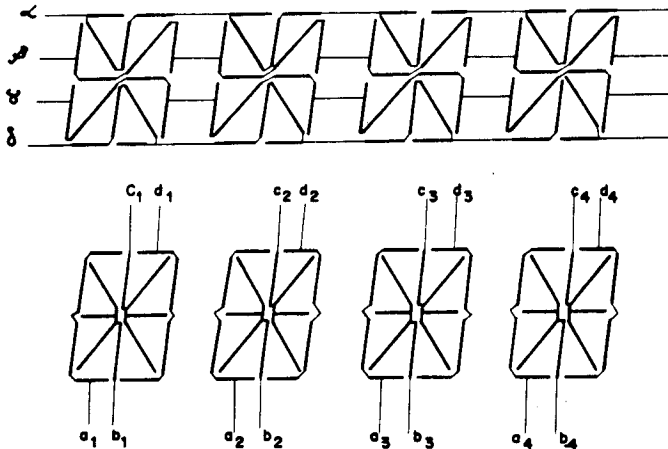
Figure 3.
The electrode patterns and the interconnections on the top and bottom plates of the display panel.

to the code necessary to address this display. The total memory required for 64 characters is $64 \times 4 \times 4 = 1024$ in the organisation 256×4. The block diagram of the system is given in figure 4. The logic circuitry required to produce the data for columns is simple and consists only of finding the number of coincidences of the column data with the addressing waveform and making a simple majority decision.
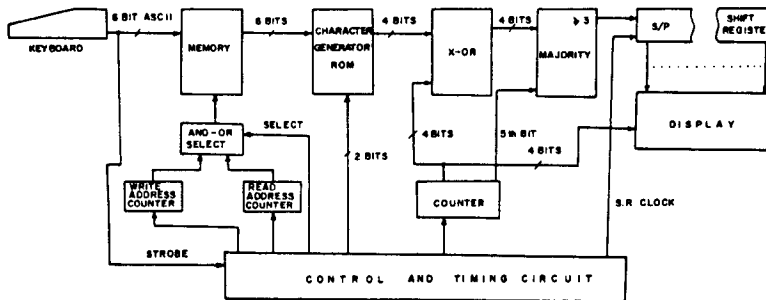

Figure 4.
Block diagram of the display system.

Photographs of some preliminary twisted nematic displays constructed on the basis of this scheme are shown in figure 5. We feel that if the display performance is optimized by a suitable choice of materials, this will be a convenient method of addressing the displays.

ACKNOWLEDGEMENT

REFERENCES
1.   P.M. Alt and P. Pleshko, *IEEE Trans*. ED-21, 146 (1974).
2.   K.G. Clark, I.A. Shanks and N.J. Patterson, *SID Digest*, p.110 (1979).