Low Voltage Driving Of STN LCDs With Low Hardware Complexity For Portable Applications

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Abstract: *In passive matrix liquid crystal displays (PMLCDs), multiplexing is achieved by using intrinsic non-linear electro-optic characteristics of the displays. Supply voltage can be reduced considerably as compared to the conventional as well as multi-line addressing techniques by using displays with steep electro-optic characteristics. The technique is demonstrated by driving a display with the hybrid addressing technique (HAT) that has a low hardware complexity. A 35% reduction in supply voltage is achieved by using a display with steeper electro-optic characteristics than necessary for the application. The technique can be extended to display gray scales in combination with the successive approximation approach by using five multiplexers and a few voltage level generators (VLG) that are common to all the drivers in the display. It is a simple solution to reduce the hardware complexity, supply voltage and cost.*

Keywords: PMLCDs; Multi-Line Addressing; Hybrid Addressing; Hardware Complexity.

Introduction

Passive Matrix Liquid Crystal Displays (PMLCDs) are popular in small and medium size display applications. Monochrome graphic and color Super Twisted Nematic (STN) LCDs are used in low cost display applications. In PMLCDs, multiplexing is achieved by using the non-linear electro-optic characteristics of the liquid crystal display. If the electro-optic characteristic is steep, then a large number of lines can be multiplexed. Supply voltage is low when the number of rows in each subgroup is equal to square root of the total number of rows in the matrix display when Multi-Line Addressing (MLA) [1-3] is used. By using liquid crystal materials with steep electro-optic characteristics than necessary for a given matrix LCD, one can reduce the supply voltage considerably. Kuijk *et.al.*,[4] showed the possibility of reducing the supply voltage when MLA technique is used along with steep electro-optic characteristics materials. Supply voltage can be further reduced by using multiple line addressing techniques like Hybrid Addressing Technique (HAT) [5], Improved Hybrid Addressing Technique-S3 (IHAT-S3) and Improved Hybrid Addressing Technique-S4 (IHST-S4) [6]. These techniques have lower hardware complexity of the column driver. Selection ratios of these addressing techniques are lower than the maximum value because of the restrictions imposed on the number of voltage levels in the column waveforms. A lower selection ratio is not a problem since the electro-optic characteristics of the liquid crystal material is steep enough for the given applications. An analysis of supply voltage requirement

using liquid crystal materials with steep electro-optic characteristics than necessary is presented in reference [7]. The hybrid addressing techniques (HAT, IHAT-S3 and IHAT-S4) have a low supply voltage and low hardware complexity of the column drivers as compared to MLA.
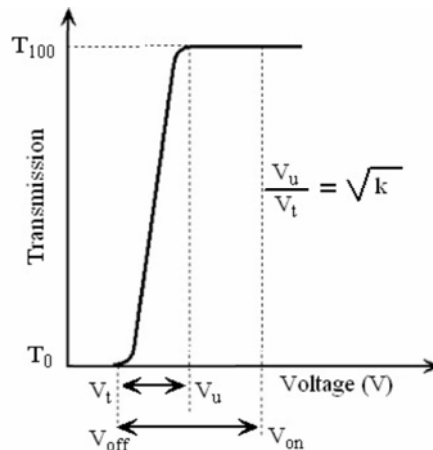

Figure 1. Electro-optic characteristics curve (Von > Vu).

Gray shades are very important in many applications. Successive Approximation Approach [8] is a better choice for displaying a large number of gray shades in PMLCDs without increasing the hardware complexity. It is important to avoid flicker while displaying large number of gray shades. We have developed a controller for driving STN LCD using HAT that has a low hardware complexity (i.e., just two voltage levels in the column waveform) and lower supply voltage. Here, development of a controller for driving 60x64 matrix STN LCDs using HAT while selecting 5 rows at a time for displaying 8 gray shades is presented.

Multiple Line Addressing Techniques

Multiple line addressing technique is a better choice for driving the STN LCDs with good brightness uniformity and contrast as compared to conventional line by line addressing technique. Supply voltage is also low but the cost of the column driver is high because more number of voltage levels are in the addressing waveform. Complexity of the column driver increases as the number of rows in each subgroup increased. HAT is a better choice for driving the STN LCDs because of the low hardware complexity.

Hybrid Addressing Technique

Number of voltage levels in the column waveforms is restricted to two levels for reducing the hardware complexity of the column driver. Number of voltage

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levels is restricted to two, three and four as compared to $(s+1)$ in the case of IHAT[1], when s rows are selected in each subgroup. In this case, the multiple-line addressing technique is referred as HAT, IHAT-S3 and IHAT-S4 respectively.
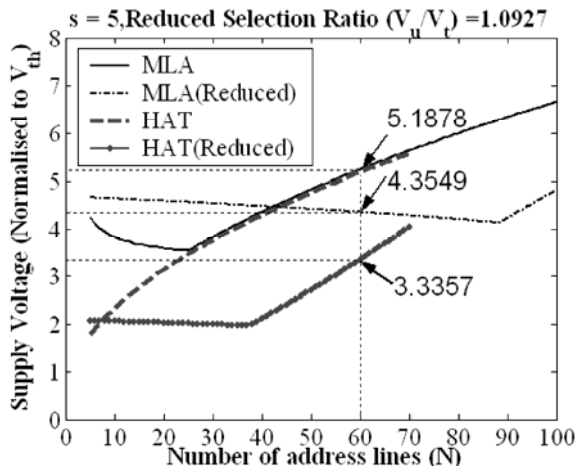
Figure 2. Comparison of supply voltage (normalized to V_{th}) for MLA and HAT when LCDs with the steep electro-optic characteristics than necessary are used.

*Driving With Low Supply Voltage and Low Hardware Complexity*

Supply voltage can be reduced if the electro-optic characteristic of the liquid crystal material is steeper than necessary [4] as shown in the Fig.1. Here the voltage across the ON pixel can be lowered to V_u without affecting the contrast of the display. Hence the selection ratio is reduced to V_u/V_t and it is referred to as reduced selection ratio. This will help to lower the supply voltage of the drive electronics without losing contrast. Low supply voltage and low hardware complexity are important for displays in portable devices. Among the multiple-line addressing techniques, HAT uses only two voltage levels in the column waveforms. We have developed a controller to demonstrate and verify our results by using STN LCDs (60X64) filled with the liquid crystal material that can be used for multiplexing 128 rows. Fig. 2 shows the supply voltage (Normalized to V_{th}) versus the number of address lines (N) while selecting 5 rows at a time ($s = 5$) in the case of HAT[5] as compared to the MLA[3] when the LCD has the liquid crystal material which is suitable for multiplexing up to 128 rows. As one see from the Fig. 2, the supply voltage is minimum i.e., just 2 (Normalized to V_{th}) for 38 rows when the liquid crystal mixture capable of multiplexing up to 128 rows is filled in the matrix LCD.

Displaying Gray Shades

A successive approximation analog-to-digital converter (ADC) uses a digital-to-analog converter (DAC) and a comparator to perform a binary search to find a digital value, which is approximately equal to the input voltage. The search tree starts with most significant bit (MSB) and ends with least significant bit (LSB). In successive approximation ADC, g comparisons are necessary in the

binary search to achieve a g-bit resolution. A similar approach is used to display gray shades in matrix LCDs[8]. To display 2^g gray shades, g frames are used and in each frame both row and column voltages are reduced by a factor $k_f = \left(\dfrac{1}{\sqrt{2}}\right)$. Wherein f corresponds to bit and it has a range of $0 \le f \le (g-1)$, when the display is scanned by using most significant bit to the least significant bit. Voltages corresponding to one of the gray shades are applied during a successive frame. In each frame the data is considered to be +1 or −1 for logic 0 or logic 1, respectively of the gray shade bit used for scanning the frame. This method can be used to display gray shades using line by line [9] as well as multi-line addressing techniques [8]. Frame response can be suppressed when multiple line addressing technique is used. In multiple line addressing technique the number of voltage levels in the row and column waveforms are three and $(s+1)$ respectively. Where, s is the number of rows in each subgroup. The number of voltage levels in any one frame is same as that of multiple-line addressing technique. The voltages necessary for row and column waveforms for the g frames are generated in voltage level generators (VLGs). Analog multiplexers are used to select the voltages corresponding to each frame. These multiplexers are common to the both row and column drivers as shown in the Fig. 3. Hence, the row and column drivers that are used to display bi-level images can be used for displaying gray shades using successive approximation approach. The hardware implementation of HAT is presented in the next sections.
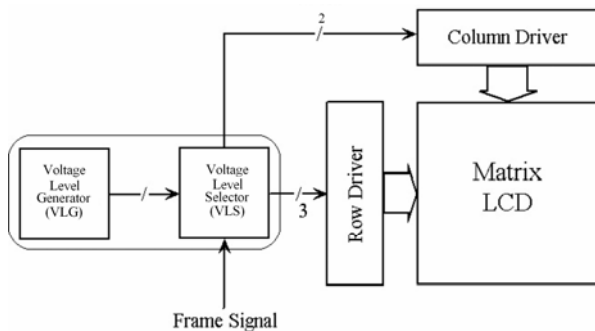
Figure 3. Schematic of the modification done outside the row and column drivers for displaying gray shades based on SAA using HAT.

Hardware Implementation

The low hardware complexity and reduced supply voltage is demonstrated with a 60X64 matrix STN LCD that is scanned by selecting five rows at a time using Hybrid Addressing Technique (HAT). Fig. 4 shows the block diagram of the HAT for displaying gray shades using successive approximation approach. Here data to be display is stored in the memory (EPROM). Control logic is used to generate the control signal to synchronize the various blocks like row select pattern generator, voltage level selector, column signal generator, subgroup sequencer and shift and latch pulses for the row and column drivers.
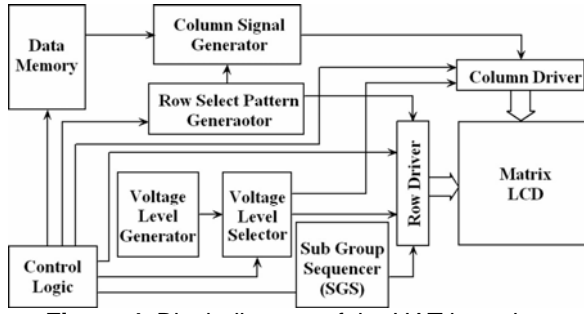
Figure 4. Block diagram of the HAT based on successive approximation approach.

The row voltages $+V_r$, 0, $-V_r$ and column voltages $+V_c$ and $-V_c$ and the scaled voltages (by a factor $2^{-1/2}$ i.e., to display gray shades) are derived from the Voltage Level Generators (VLG). In Fig. 4 the voltage level selector is used to implement the successive approximation approach to display gray shades by selecting the corresponding voltages which are generated in VLG. The selection ration of HAT is maximum when $\left(V_r/V_c\right) = \sqrt{N/s}$. If the electro-optic characteristics liquid crystal mixture is steeper than necessary, then the *rms* voltage across the ON and OFF pixels can be adjusted by modifying the row and column voltage levels. In this case the V_r and V_c are modified [7] according to the equation (1).

$$\frac{V_r}{V_c} = \frac{\beta}{2\alpha}\left(\frac{k+1}{k-1}\right) \pm \sqrt{\left[\frac{\beta}{2\alpha}\left(\frac{k+1}{k-1}\right)\right]^2 - \frac{\gamma}{\alpha}} \qquad (1)$$

Where, $\alpha = 2^s$, $\beta = 2\left(4\left(\sum_{i=0}^{(s-1)/2} \frac{(s-1)!}{i!(s-i-1)!}\right) - 2^s\right)$,

$\gamma = 2^s\left(\frac{N}{s}\right)$ and $k = \left(\frac{V_u}{V_t}\right)^2$

The supply voltage is determined by the maximum swing in the addressing waveforms. The expressions for the supply voltage to display bi-level image are

$$V_{sup} = 2x\sqrt{\frac{\delta}{\alpha\,x^2 - \beta\,x + \gamma}}\ V_{th} \qquad \text{for } (V_r \geq V_c)$$

$$V_{sup} = 2\sqrt{\frac{\delta}{\alpha\,x^2 - \beta\,x + \gamma}}\ V_{th} \qquad \text{for } (V_r \leq V_c)$$

Where $\delta = 2^s\left(N/s\right)$ and $x = \left(V_r/V_c\right)$

As an example, we consider a display with N=60, V_t=1.0V and an STN display with multiplexing ratio of 128 rows. In this case the row to column voltage ratios and supply voltages are given in Table 1.

Table 1.

Technique	V_r	V_r/V_c	V_{sup} (Norm. to V_{th})
MLA	2.6248	1.5492	5.2495
MLA-R	1.3359	0.6135	4.3549
HAT	2.5939	3.4641	5.1878
HAT-R	1.6679	1.7932	3.3357

Supply voltage increases with g that is when 2^g gray shades are displayed. It is increases by a factor $\sqrt{\dfrac{g\,2^{(g-1)}}{2^g - 1}}$ as compared to the bi-level display. This scaling factor is independent of the addressing technique used to scan the display. In order to display gray shades using SAA, scaled row and column voltage levels are generated using voltage divider network. Three voltage level generators with the scaling factors K_f are generated while scanning the display in three successive frames as shown in Fig. 5. Analog multiplexers are used to select one of the VLGs corresponding to each frame (i.e., using 3:1 analog multiplexers) using frame signal generated in control logic to select the voltages for the row and column drivers as shown in Fig. 3. All the necessary control signals are implemented using Complex Programmable Logic Device (CPLD). In our design we used Altera CPLD EPM7128LC84-15. The row driver has been designed to support the 60X64 matrix STN LCD to scan the display by selecting five rows at a time. The commercially available column driver (LC7940ND) is used to support the two voltage level at the column waveforms.
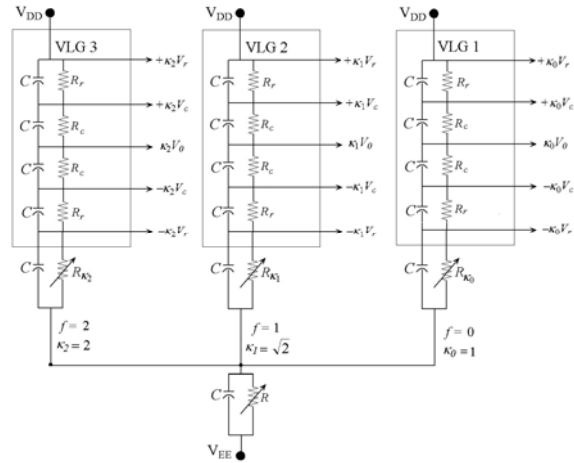
Figure 5. Schematic block diagram of the VLGs corresponding to the three frames.

Results and Conclusions

The HAT has low hardware complexity (two voltage levels in the column waveforms and three voltage levels in the row waveforms) and has the lowest supply voltage for lower values of *N*. Fig. 8(a) shows the photograph of the STN display using HAT-R, selecting 5 rows at a time. Fig. 6 shows the comparison of the *rms* voltage across the ON and OFF pixels with various supply voltage.
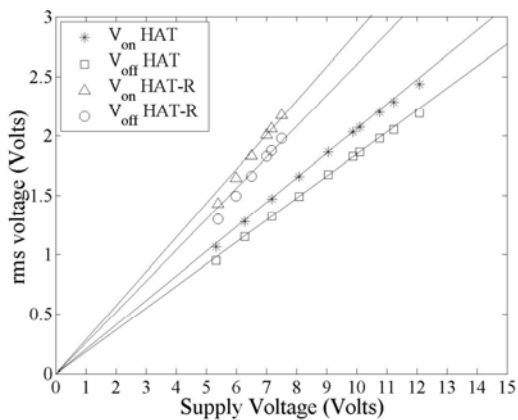
Figure 6. Comparison of *rms* voltage across the ON and OFF pixels while driving the 60X64 STN LCD using HAT and HAT-R.

From these measurements it is very clear that the supply voltage to drive the panel is lower for HAT-R as compared to HAT. The minimum supply voltage is achieved when the maximum swings in the row and column waveforms are equal. This can be achieved when one drive the panel with 38 rows using HAT-R with the liquid crystal mixture capable of multiplexing 128 rows as shown in the Fig. 2. In our design, we drive the panel with 60 rows using the STN display with multiplexing limit of 128 rows. In this case the supply voltage is 3.3357(Normalized to V_{th}), which is low as compared to MLA and HAT while selecting 5 rows at a time (Refer Fig. 2). Fig. 7 shows the waveforms of the row and column as well as the resultant waveforms across the ON pixel. Here, the row to column voltage ratio of HAT and HAT-R is 3.4641 and 1.7932 respectively. The measured peak-peak voltage of row and column voltage levels for HAT is 5.05V and 1.46V and that for HAT-R are 3.6V and 2.0V, respectively.
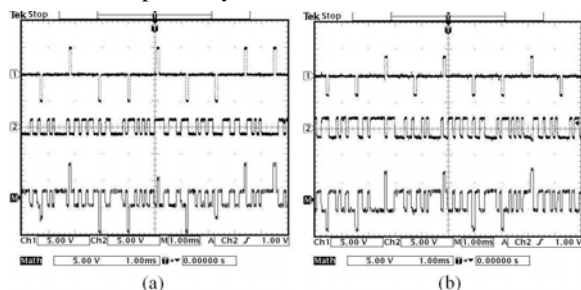
Figure 7. Comparison of Row, Column and resultant waveform across the ON pixel while using (a) HAT and (b) HAT-R.

The supply voltage is calculated according to the maximum swing in the addressing waveforms. In both the cases the row voltage is greater than column voltage. The maximum swing in the row waveforms are reduced from 10.10V in HAT to 7.20V in HAT-R. The supply voltage is calculated for both HAT and HAT-R, the reduction is around 35%. Gray shades are generated based on Successive Approximation Approach with HAT-R. Fig. 8(b) shows the photograph of STN panel displaying graphic image. Here, eight gray shades are demonstrated based on SAA using HAT-R. It is a simple

solution to reduce the hardware complexity, supply voltage and hence the cost of driving the passive matrix LCDs.
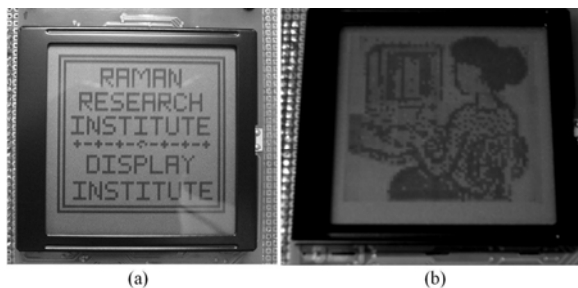
Figure 8. Photographs of the 60X64 matrix STN LCD that is addressed using (a) HAT-R (b) Graphic image with eight gray shades based on SAA in combination with HAT-R by selecting 5 rows at a time.

References
1. T N Ruckmongathan, "A Generalized Addressing Technique For RMS Responding Matrix LCDs", 1988, IDRC, pp 80-85, 1988.

2. T N Ruckmongathan, T Kuwata, T Ohnishi, S Ihara, H Koh and Y Nakagawa, "A New Addressing Technique For Fast Responding STN LCDs", Japan Display '92, pp 65-68, 1992.

3. B Clifton, D Prince, B Leybold, T J Scheffer, A R Conner and B Greenberg, "Optimum Row Functions And Algorithms For Active Addressing", SID 93 Digest, pp 89-92, 1993.

4. Karel E Kuijk, Alex V Henzen, Reinder Smid, "Minimum-Voltage Driving of STN LCDs by Optimized Multiple-Row Addressing", Proceedings of Eurodisplay, pp 77-80, 1999.

5. T N Ruckmongathan and N V Madhusudana, "New Addressing Techniques For Multiplexed Liquid Crystal Displays", Proceedings of the SID, Vol.24, No.3, pp 259-262, 1983.

6. T N Ruckmongathan, "An Addressing Technique With Reduced Hardware Complexity", SID 94 Digest, pp 65-68, 1994.

7. K G Panikumar and T N Ruckmongathan, "Driving passive matrix LCDs with low hardware complexity and reduced supply voltage", Journal of the SID, Vol.10, No.4, pp.363-373, 2002.

8. K G Panikumar and T N Ruckmongathan, "Displaying Gray Shades In Passive Matrix LCDs Using Successive Approximation", Proceedings of the 7th Asian Symposium on Information Display (ASID'02), 229-232, 2002.

9. T N Ruckmongathan, "Displaying Gray Shades in Liquid Crystal Displays", Pramana, Vol. 61, No. 2, pp 313-329, 2003.